WHAT IS CLAIMED IS:

1. A method for designing a semiconductor integrated circuit device including a plurality of blocks, the method comprising the steps of:

a) defining exclusive operation information among the blocks;

b) defining interconnection information about a sharable resource within each said block; and

c) extracting a resource sharable among the blocks based on the information about the sharable resource and the exclusive operation information among the blocks.

2. The method of Claim 1, further comprising the step of d) generating interconnection information about the resource sharable among the blocks after the step c) has been performed.

3. The method of Claim 2, further comprising the step of defining timing information about the sharable resource within each said block before the step d) is performed,

wherein in the step d), the timing information is used.

4. The method of Claim 2, further comprising the step of e) generating interconnection information about an optimized top-level hierarchy based on the interconnection information

about the resource sharable among the blocks and interconnection information about a top-level hierarchy that has been generated in advance.

5. The method of Claim 2, further comprising, before the step d) is performed, the steps of:

defining a standard interface for the sharable resource; and

generating information about the standard interface for the sharable resource,

wherein in the step d), the standard interface information is used.

6. A method for designing a semiconductor integrated circuit device including a plurality of blocks and a resource shared among the blocks, each said block including a plurality of cells, the method comprising the steps of:

a) defining exclusive operation information among the blocks; and

b) generating a signal switching control for the resource shared among the blocks based on the exclusive operation information.

7. The method of Claim 6, further comprising the step c) of defining interconnection information about a top-level hi-

erarchy and generating interconnection information about an optimized top-level hierarchy after the step b) has been performed.

8. A method for designing a semiconductor integrated circuit device including a plurality of blocks, each including a plurality of cells, the method comprising the steps of:

a) defining exclusive operation information as to each functional unit within each said block;

b) defining interconnection information about a top-level hierarchy; and

c) generating a power management for each said block based on the exclusive operation information and the interconnection information about the top-level hierarchy.

9. The method of Claim 8, further comprising the step d) of generating interconnection information about an optimized top-level hierarchy based on the interconnection information about the top-level hierarchy and the power management after the step c) has been performed.

10. A method for designing a semiconductor integrated circuit device including a plurality of blocks, each including a plurality of cells, the method comprising the steps of:

a) defining exclusive operation information among the

blocks;

b) defining interconnection information about a top-level hierarchy; and

c) generating a power management among the blocks based on the exclusive operation information and the interconnection information about the top-level hierarchy.

11. The method of Claim 10, further comprising the step d) of generating interconnection information about an optimized top-level hierarchy based on the interconnection information about the top-level hierarchy and the power management after the step c) has been performed.

12. A method for designing a semiconductor integrated circuit device including a plurality of blocks, each including a plurality of cells, the method comprising the steps of:

a) defining priority-order information as to respective functional units within each said block;

b) defining interconnection information about a top-level hierarchy;

c) generating priority-order-controlling information for the respective blocks based on the priority-order information as to the respective functional units within each said block and the interconnection information about the top-level hierarchy;

d) defining information about allowable power; and

e) generating a power management based on the priority-order-controlling information for the respective blocks such that each said cell operates within a range of the allowable power defined by the allowable power information.

13. The method of Claim 12, further comprising the step f) of generating interconnection information about an optimized top-level hierarchy based on the interconnection information about the top-level hierarchy and the power management after the step e) has been performed.